What is claimed is:

1. A method for fabricating a semiconductor device having a first region and a second region, comprising the steps of:

forming a plurality of conductive patterns on a substrate in the first region and the second region, wherein each of the conductive patterns includes sequentially stacked layers of a conductive layer and a hard mask;

removing the hard mask in the second region to expose the conductive layer;

forming a diffusion barrier layer on the exposed conductive layer;

depositing an insulation layer on the entire resulting substrate structure in the first region and the second region;

selectively etching the insulation layer in the second region to form an opening exposing the diffusion barrier layer; and

forming a conductive wire electrically connected to the diffusion barrier layer through the opening.

2. The method as recited in claim 1, wherein the first region is a cell region of a semiconductor memory device and a second region is a peripheral region of the semiconductor memory device.

3. The method as recited in claim 2, wherein the

conductive pattern is a bit line pattern.

4. The method as recited in claim 1, wherein the diffusion barrier layer uses at least any material selected from a group consisting of Ti, TiN, TiW, Ta and TaN.

5. The method as recited in claim 1, wherein the hard mask is made of a nitride-based material.

6. The method as recited in claim 1, wherein the conductive wire is made of any material selected from a group consisting of Al, Cu, Ag, Au or W.

7. The method as recited in claim 1, wherein the conductive wire is a metal wire for connecting a power line to the conductive layer and the opening is a via hole.

8. The method as recited in claim 7, wherein the metal wire is substantially connected to an upper part of the conductive layer and an active region of the substrate in addition to the electrical connection of the conductive metal wire to the diffusion barrier layer.